

App. Serial No. 10/528,753
Docket No.: FR 020101 US

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Remarks

Claims 1-9 are currently pending in the patent application. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

The non-final Office Action dated July 12, 2006 indicated a request to address informalities in the specification, that the application title is not descriptive, that the related patent information should be updated, and listed the following rejections: claims 1-9 stand rejected under 35 U.S.C. § 112(2); claims 1-5 and 7-9 stand rejected under 35 U.S.C. § 102(b) over Robert (U.S. 5,902,152); and claims 1-3 and 5-9 stand rejected under 35 U.S.C. § 102(e) over Panella *et al.* (U.S. 6,853,559).

Applicant has amended the specification as indicated on page 3 of this response to address informalities.

Regarding the application title, Applicant believes that the title is descriptive of the claimed invention as required by M.P.E.P. § 606. The application title (*i.e.*, CONNECTOR FOR CHIP-CARD) is descriptive of the claimed invention which is directed towards a connector with upper and lower surfaces and contact pins to contact a chip card.

Regarding the related patent information, Applicant submits that a related patent document section should not be required, as the instant application priority chain has been officially recognized as a national stage application under 35 U.S.C. § 371; this data appears on the coversheet of the published patent application. Notwithstanding, Applicant has amended the specification to indicate related patent information, and requests that the objection be removed.

Applicant respectfully traverses the Section 112(2) rejections of claims 1-9 because the claimed limitations are clear, in that one of ordinary skill in the art would readily understand the limitations, as is supported by the specification in the figures and description, and as otherwise understood in the art. In particular, the basis for the Examiner's rejection is that Applicant's use of the term "intended to be" renders the claims indefinite and the term does not recite positive structure. Applicant contends that "intended to be" is clear and has come to be a commonly used term in claiming an invention. A brief review of the U.S. Patent Office's own database, a multitude of issued patents indicate the term "intended to be" in claims. Here, such language refers, for

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certain embodiments (and by illustrative example), to subject matter applicable to the structure of a connector. In view of the foregoing, Applicant contends that the scope of the claims is ascertainable and therefore the Section 112(2) rejections should be withdrawn.

Notwithstanding the above discussion, in an effort to facilitate prosecution, Applicant has amended claims 1 and 2 in a manner consistent with the claims as filed and with Section 112(2). Specifically, Applicant has removed the phrase "intended to be" from the claims. Applicant notes that the amendments are not being made to overcome any issues of patentability raised by the rejections in the Office Action. The claims are patently distinguishable over the cited references for the reasons discussed below. Therefore, Applicant requests that the Section 112(2) rejections be withdrawn.

Applicant traverses all of the claim rejections relying upon the Robert reference because the rejections are unclear in that the figures 10 and 11 are recited, yet the Robert reference includes only figures 1-6. As is consistent with the M.P.E.P. and 35 U.S.C. §132, the claim rejections should recite portions of a reference in a manner that apprises the Applicant of the nature of the rejection and the cited art relied upon in making the rejection; in this instance, the citation to nonexistent figures fails to do so. Should the rejections be maintained, Applicant requests clarification and an opportunity to respond thereto.

Applicant further traverses the Section 102(b) rejections of claims 1-5 and 7-9 because the cited portions of the Robert reference fail to correspond to all of the claimed limitations. For example, regarding independent claims 1 and 2, the Office Action fails to cite any portion of the Robert reference that corresponds to claimed limitations directed to a connector having a cavity in its upper surface, or to limitations directed to contact pins that are connected to contact surfaces and emerge below a lower surface to contact a board. While the Office Action refers to portions of the Robert reference when discussing these limitations, there is no showing of correspondence with the claimed limitations in a manner commensurate with Section 102. The following more particularly discussed this lack of correspondence.

Regarding claimed limitations directed to a cavity, the Office Action cites to a support 2 that has an upper surface 4 and a lower surface 6 as the claimed connector (see,

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e.g., Fig. 1 and col. 2, lines 59-67), and cites an area in which component 1 sits as the cavity. However, these cited portions do not correspond to the claimed limitations; specifically, the area in which component 1 sits is below the lower surface 6 of the support 2. In this regard, the rejection fails to assert a cavity as claimed and/or, for example, to show how the asserted cavity in the Roberts reference could function as the claimed cavity (*e.g.*, as providing connection to an underlying board and/or for accepting and connecting to a circuit).

In attempting to show correspondence to the claimed limitations directed to contact pins and their related connectivity, the Office Action cites to contact terminals 3, but fails to show any contact pins that emerge below a lower surface to contact a board and connect to contact surfaces of the cavity. Generally, the Office Action presents a confusing rejection by referring to the chip card 20 as both a chip card as described in the Roberts reference and as a board to which contact pins extending below a lower surface of a connector couple (see page 4 of the Office Action). In this regard, the Office Action has failed to show correspondence to the claimed limitations directed to contact pins connected to contact surfaces of a cavity, including such contact pins that emerge below a connector's lower surface to contact a board. Moreover, the Robert reference teaches that contact terminals 3 project above the upper plane 4 in order to be in electrical contact with the contact areas 5 of the chip card (see, *e.g.*, Abstract), thus failing to teach contact terminals (*e.g.*, 3) that emerge below a lower surface to contact a board as in the claimed invention.

In view of the above, the Robert reference does not teach a connector as claimed, having either a cavity in the upper surface thereof or contact pins arranged as claimed. Accordingly, the Section 102(b) rejections of independent claims 1 and 2, as well as the rejections of claims 3-5 and 7-9 that depend from claim 1, are improper and Applicant requests that they be withdrawn. Notwithstanding the impropriety of the rejections of all of the dependent claims as related to the independent claims above, the limitations of certain dependent claims are addressed further below.

Applicant traverses the Section 102(b) rejections of claims 3 and 7-9 because the Office Action fails to cite any portion of the Robert reference in support of these rejections. For example, the Office Action has failed to show any teaching or suggestion

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of a cavity bounded by contact pins, of a chip card reader, a mobile telephone or a personal digital assistant. As consistent with the M.P.E.P. and relevant case law, a Section 102 rejection should recite portions of a reference in a manner that apprises the Applicant of the nature of the rejection and the cited art relied upon in making the rejection. In this instance, the citation is to an entire patent document, thus failing to recite the claim rejections with any specificity. In this regard, the rejections of claims 3 and 7-9 are also improper for these reasons and should be removed.

Applicant traverses the Section 102(e) rejections of claims 1-3 and 5-9, because the cited portions of the Panella reference fail to correspond to all of the claimed limitations. Regarding independent claims 1 and 2, the Office Action fails to cite any portion of the Panella reference that corresponds to claimed limitations directed to the cavity comprising contact surfaces connected to the contact pins and to contact the contact tabs. The Office Action fails to cite to any portion of the Panella reference as being the contact surfaces of the claimed invention. In addition, the Office Action cites to "58" and "232" of Panella as "contact tabs" (see, *e.g.*, page 5, last paragraph); however, 58 and 232 are both part of IC 22 and do not contact anything outside of the IC (see, *e.g.*, Fig. 23 and related discussion).

Moreover, the Office Action cites to PCB 114 of Fig. 23 as both the chip card and the board in the claimed invention. The Office Action has not shown, and Applicant fails to see, how PCB 114 corresponds to a chip card as in the claimed invention.

The Office Action further fails to cite any portion of the Panella reference that corresponds to claimed limitations directed to contact pins emerging above an upper surface of a connector to contact a chip card. While the Office Action cites to several items found in Fig. 23 of the Panella reference (*i.e.*, 228, 24, 116 and 242), none of these cited elements are contact pins as in the claimed invention because none of them contact a chip card. Specifically, power pad 228 is part of IC 22 and, as such, does not emerge above the upper surface of connector 112 and it does not contact PCB 114 as asserted by the Office Action (see, *e.g.*, col. 45, lines 14-55).

The remaining portions of the Panella reference cited by the Office Action concern two different methods of delivering power to IC 22 via power contacts 92 located on the sides 72 and 74 of the IC, and are unrelated to the claimed limitations and

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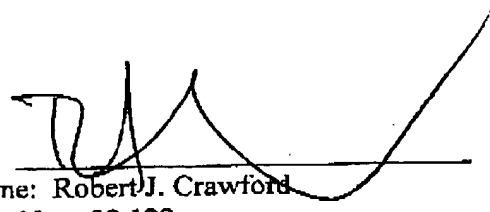
do not function as suggested in the Office Action. Power is delivered to the power contacts 92 located on side 72 (right side of Fig. 23) of IC 22 via a power connection 24, formed as a conductor 116 and connector 112 is electrically coupled to the power contacts 92 via corresponding power contacts 242 carried by the connector 112. See, e.g., col. 46, lines 8-16. The power connection 24 on side 72 of IC 22 emerges above the upper surface of connector 112, but the power connection 24 does not contact PCB 114 as asserted by the Office Action. Alternatively, power is delivered to the power contacts 92 on side 74 (left side of Fig. 23) of the IC 22 via the power connection 24, formed as a PCB trace 116 on the PCB and formed as a conductor 116 carried by the connector 112. See, e.g., col. 46, lines 10-13. The power connection 24 on side 74 of the IC 22 does contact the PCB 114, but the power connection 24 does not emerge above the connector 112 as asserted by the Office Action. In this regard, these portions of the Panella reference do not correspond to the claimed limitations.

In view of the above, the circuits in the Panella reference is clearly different than the claimed limitations, and the cited portions of the Panella reference do not correspond to the claimed limitations, such as those directed to subject matter including contact pins that both emerge above the upper surface of a connector to contact a chip card. Accordingly, the Section 102(e) rejections of claims 1-3, 5-9 are improper and Applicant requests that they be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the attorney overseeing the application file, Adam L. Stroud, of Philips Corporation at (408) 474-9064.

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